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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/006,157	12/10/2001	Igor Taranov	J141 0002	9698
20985	7590	04/10/2006	EXAMINER	
FISH & RICHARDSON, PC P.O. BOX 1022 MINNEAPOLIS, MN 55440-1022			TRUONG, LAN DAI T	
			ART UNIT	PAPER NUMBER
			2143	

DATE MAILED: 04/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/006,157

Applicant(s)

TARANOV, IGOR

Examiner

lan dai thi trung

Art Unit

2143

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 January 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-26 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-26 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date <u>02/06/06</u> | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. This action is response to communications: application, filed 12/10/2001; amendment filed 01/23/2006. Claims 1-26 are pending; claims 1-2, 23-24 and 25 are amended

Response to Arguments

2. Applicant's argument filed 01/23/2006 has been fully considered, but they are moot in view with new ground for rejection

Claim rejections-35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 1, 19, 21, 23 and 25 are rejected under 35 U.S.C 103(a) as being unpatentable over Tavana et al. (U.S. 2002/0024973) in view of Clark et al. (U.S. 6,075,773)

Regarding to claim 25, which is exemplary with claims 1, 19 and 23:

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Tavana discloses the invention substantially as claimed, including a apparatus, which can be implemented in computer hardware or software code for dispatching bursts of packets onto a computer network, comprising:

The program memory comprising test packet sequencer software comprising a series of instructions executable by the processor under control of an operating system, the instructions, if executed by the processor, causing the processor to:

Establish a first I/O completion port: (Tavana discloses “PHY 24:1” which is equivalent to “a first I/O completion port”: abstract, lines 1-13; figure 1; [0002])

generate a plurality of test packets: (Tavana : abstract, lines 1-13; figure 1; [0002])

forward to the first I/O completion port a request that the test packets be dispatched; and, dispatch the test packets onto the network by way of the network interface under control of the first I/O completion port: (Tavana : abstract, lines 1-13; figure 1; [0002])

measure departure time of each of the test packets; and measure return time of each of the test packets: (Tavana : abstract, lines 1-13; figure 1; [0002])

A network interface: (Tavana: figure 1; items 22:1, 24:1; [0002])

However, Tavana does not explicitly disclose a computer processor, see (Clark discloses a packet generating ethernet testing device comprises “a microprocessor” which is equivalent to “A computer processor”: abstract, liens 1-5)

A program memory accessible to the processor, see (Clark discloses a packet memory for storing the generated test packets. Clark also discloses the interacting between the processor and packet memory: abstract, lines 1-20; column 4, lines 45-60)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Clark's ideas of incorporating processes of a processor which generates and dispatches test packets into network and a memory used to store test packets with Tavana's system in order to be able provide an efficiency network diagnostic system

Regarding to claim 21:

In addition to rejection in claims 1 and 3, Tavana-Clark further discloses receiving returning dispatched test packets after they have traversed a path in the network and time stamping notifications that the packets have been received: (Tavana : abstract, lines 1-13; figure 1; [0002])

Claim 2 is rejected under 35 U.S.C 103(a) as being un-patentable over Tavana-Clark in view of VanDervort (U.S 5,812,528)

Regarding to claim 2:

Tavana-Clark discloses the invention substantially as disclosed in claim 1, but does not explicitly teach wherein the packets are forwarded to the I/O completion port asynchronously

However, VanDervort discloses a method of measuring "test cell" which is equivalent to "test packets" round trip time within an "ATM communication network " which is shared functionality with "forwarding to the I/O completion port asynchronously"(abstract: lines 1-16; column 1, lines 23-29)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine VanDervort's ideas of rounding of test cells in an asynchronous transfer mode with Tavana-Clark's system in order to provide flexibility of network configuration and implementation, see (VanDervort: column 2, lines)

Claims 3-10, 17, 22 and 26 are rejected under 35 U.S.C 103(a) as being unpatentable over Tavana-Clark in view of McKee et al. (U.S. 5,477,531)

Regarding to claims 3-4, which are exemplary with claims 5-7, 17:

Tavana-Clark discloses the invention substantially as disclosed in claim 1, but does not explicitly teach wherein forwarding the test packets to the I/O completion port is performed by a user mode thread during a single time slice; before forwarding the test packets, terminating the current time slice for the user thread; and forwarding the test packets to the I/O completion port at a start of a next time slice for the user thread

However, McKee discloses a plurality of test packet in one burst are in the same “duration” which is equivalent to “time slice.” McKee also discloses one burst of a plurality of test packets has subsided before the next burst is sent, this process is shared functionality with “forwarding the test packets to the I/O completion port at a start of a next time slice for the user thread”: McKee: column 8, lines 40-42; column 9, lines 23-25)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine McKee’s ideas of using single time slice to process test packet with Tavana-Clark’s system in order to send out sequences of test packets to the target station, see (McKee: column 4, lines 8-12)

Regarding to claim 26:

Tavana-Clark discloses the invention substantially as disclosed in claim 25, but does not explicitly teach wherein the test packet sequencer software comprises a test controller layer associated with a second I/O completion port and a command controller layer associated with the first I/O completion port, wherein the test controller layer is configure to pass commands to the

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command controller layer by way of the first I/O completion port and the command controller layer is configured to pass raw data to the test controller layer by way of the second I/O completion port

However, McKee discloses “a test sequence program” which is equivalent to “test packet sequencer software” utilizes the services provided by the protocol stack 14 to send a test packet over network. The test sequence program controls the transmission of a test packet to the specified remote station using the protocol stack 14. So it means the test sequence program must receive “request for testing” or command. Then the test packets must be generated and transmits to the destination.

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine McKee’s ideas of using test sequence program to control transmission test packets with Tavana-Clark’s system in order to send out sequences of test packets to the target station, see (McKee: column 4, lines 8-12)

Regarding to claims 8-10, 22

In addition to rejection in claim 3, Tavana-Clark- McKee further discloses receiving returning dispatched test packets after they have traversed a path in the network and time stamping notifications that a packets have been received: (Tavana: abstract, lines 1-13; figure 1; [0002])

Claims 18 and 24 are rejected under 35 U.S.C 103(a) as being un-patentable over Tavana-Clark further in view of Ranmanathan et al. (U.S 6,076,113)

Regarding to claims 18 and 24:

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Tavana-Clark discloses the invention substantially as disclosed in claim 1, but does not explicitly teach wherein generating the test packets comprises generating a plurality of equal-sized test packets

However, Ranmanathan discloses equal size packets to emulate the TCP's transport information, see (Ranmanathan: column 2, lines 33-35)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Ranmanathan's ideas of using equal size packets with Tavana-Clark's system in order to emulate the TCP's transport information, see (Ranmanathan: column 2, lines 33-35)

Claim 20 is rejected under 35 U.S.C 103(a) as being un-patentable over Tavana-Clark -Ranmanathan in view of Crayford et al. (U.S. 6,016,308)

Regarding to claim 20:

Tavana-Clark -Ranmanathan discloses the invention substantially as disclosed in claim 18, but does not explicitly teach wherein each of the test packets has a size in the range of 46 bytes to 1500 bytes

However, Crayford discloses Ethernet standards packet size is in range of 46 bytes to 1500 bytes, see (Crayford: column 2, lines 6-30)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Crayford's ideas of using packet size in range of 46 bytes to 1548 bytes with Tavana-Clark -Ranmanathan's system in order to indicate a standard frame of data to be sent over the network, see (Crayford: column 2, lines 1-30)

Claim 11 is rejected under 35 U.S.C 103(a) as being un-patentable over Tavana-Clark- McKee further in view of Johnson, Jr. (U.S. 5,640,504)

Regarding to claim 11:

Tavana-Clark- McKee discloses the invention substantially as disclosed in claim 9, but does not explicitly teach maintaining a private heap for packet data, wherein the private heap is accessible to the user mode thread

However, Johnson discloses method of storing “the receiving information” which is equivalent to “returned test packet” into heap, see (Johnson: column 2, lines 12-19)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Johnson’s ideas of using heap for storing test packets with Tavana-Clark- McKee’s system in order to routing information see (Johnson: column 2, lines 12-15)

Claims 12-16 are rejected under 35 U.S.C 103(a) as being un-patentable over Tavana-Clark- McKee-Johnson Jr. in view of Garber et al. (U.S. 5,699,539)

Regarding to claims 12-14:

Tavana-Clark- McKee-Johnson Jr. discloses the invention substantially as disclosed in claim 11, but does not explicitly teach wherein the private heap comprises standard-size allocation units for storing packets; wherein the standard-size allocation units are of an operating system memory page size; wherein the standard-size allocation units are 4096 bytes

However, Garber discloses a heap comprises allocation units for storing data. The allocation unit has size of 4096 bytes, see (Garber: column 1, lines 60-67; column 2, lines 48-54)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Garber's ideas of using heap comprise 4096 bytes allocation units with Tavana-Clark- McKee-Johnson Jr.'s system in order to provide compressing page, see (Garber: column 2, lines 48-54)

Regarding to claims 15-16:

Tavana-Clark- McKee-Johnson Jr. discloses the invention substantially as disclosed in claim 11, but does not explicitly teach assigning a larger than default process working set size to the user mode thread; wherein the process working set size exceeds 8 Mbytes.

However, Garber discloses computer system with working set standard size of 8 Mbytes can take care process working set size of 16 Mbytes, see (Garber: column 1, lines 45-50)

Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to combine Garber's ideas of assigning a larger than default process working set size to the user mode thread with Tavana-Clark- McKee-Johnson Jr.'s system in order to compress data, see (Garber: abstract, lines 1-27)

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to lan dai thi truong whose telephone number is 571-272-7959. The examiner can normally be reached on monday- friday from 8:30am to 5:00 pm.

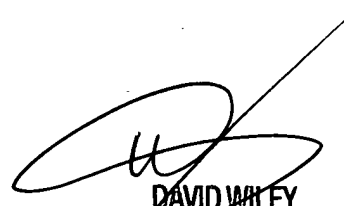
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Wiley can be reached on (571) 272-3923. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lan Dai Thi Truong
Examiner
Art Unit 2143

Ldt
03/29/2006



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